WHAT IS CLAIMED IS:

1. A phase change memory cell fabricated by integrated circuit techniques on a semiconductor substrate, comprising:

an insulating, dielectric layer on the substrate;

a thin conductive film on the dielectric layer, the plane of the film being generally parallel to the plane of the substrate;

a layer of a phase change material supported by the dielectric layer; and

an electrically resistive interface between the thin conductive film and the phase change material layer, the interface being defined by an area of engagement between the film and the layer that is generally normal to the plane of the substrate.

2. The memory cell of Claim 1, wherein:

the electrical resistance of the interface is inversely proportional to the area of engagement; and

the width of the conductive film generally parallel to the plane of the substrate and the height of the conductive film generally normal to the plane of the substrate determine the area of engagement.

3. The memory cell of Claim 2, wherein the width of the conductive film generally parallel to the plane of the substrate is determined by photolithography and the height of the conductive film generally normal to the plane of the substrate is determined by deposition parameters.

4. The memory cell of Claim 3, wherein heat produced by current through the interface flows from the interface into the phase change material layer in a direction generally parallel to the plane of the substrate.

5. The memory cell of Claim 4, which further comprises a contact on the phase change material layer, wherein:

a current path from the interface into the phase change material layer lies in a direction substantially parallel to the plane of the substrate; and

a current path from the phase change material layer into the contact lies in a direction generally normal to the plane of the substrate.

6. The memory cell of Claim 1, wherein the phase change material layer and the thin conductive film are not relatively superjacent or subjacent.

7. The memory cell of Claim 6, wherein the phase change material layer resides in a trench formed in the dielectric layer, the bottom surface of the trench and the phase change material layer being coplanar with or below the lower surface of the dielectric layer.

8. The memory cell of Claim 7, further comprising a transistor formed in and on the substrate and in the dielectric layer, and wherein an output of the transistor is electrically continuous with one terminus of the thin conductive film, the other terminus of the thin conductive film engaging the dielectric layer to define the interface.

9. The memory cell of Claim 8, wherein the transistor is a MOSFET having a gate, wherein the thin conductive film is generally coplanar with a gate electrode of the gate.

10. The memory cell of Claim 9, wherein:

the dielectric layer comprises a first, lower stratum, a second intermediate stratum on the first stratum and a third, upper stratum on the second stratum;

the gate electrode and the conductive layer reside on the first stratum, in the second stratum and under the third stratum; and

the phase change material layer resides on the first stratum and in the second and third strata.

11. The memory cell of Claim 10, further comprising:

a contact on the gate electrode; and

a topmost stratum on the third stratum, wherein the contact on the phase change material layer and the contact on the gate electrode reside in the topmost stratum.

12. A method of fabricating a phase change memory cell on a substrate by integrated circuit techniques, comprising:

forming a thin conductive film on a first dielectric stratum on the substrate, the film being generally parallel to the plane of the substrate; and

forming a layer of a phase change material on the first stratum so that a terminus of the film and a terminus of the phase change material layer have an area of engagement therebetween, the area of engagement being generally normal to the plane of the substrate, and an electrically resistive interface being defined by the area of engagement.

13. The method of Claim 12, wherein the electrical resistance of the interface is inversely proportional to the area of engagement, and which further comprises:

selecting the width of the film parallel to the plane of the substrate and the height of the film normal to the plane of the substrate to determine the area of engagement.

14. The method of Claim 13, wherein the width of the film is determined by photolithography and the height of the film is determined by thin film deposition parameters.

15. A method of fabricating a phase change memory cell on a generally planar semiconductor substrate bearing a generally planar ILD layer, comprising:

depositing a thin film of a conductive material on a bottom electrode free surface within the ILD layer, the thin film being generally parallel to the plane of the substrate and having a first terminus;

forming a first generally planar IMD layer over the free surface of the thin film;

defining a second terminus of the thin film by forming a trench through the first IMD layer and the thin film; and

filling the trench with a phase change material, a side portion of which has a generally planar interface with the second terminus of the thin film, the plane of the interface being generally normal to the plane of the substrate.

16. The method of Claim 15, further comprising a first electrode within the ILD layer, wherein the thin film is deposited so that its first terminus is in contact with the first electrode.

17. The method of Claim 15, wherein the trench is formed partially into the ILD layer.

18. The method of Claim 15, wherein heat produced at the interface by the flow of current therethrough flows into the phase change material in a direction generally parallel to the plane of the substrate.

19. The method of Claim 18, wherein the conductive material comprises a high bandgap and thermal conductivity material.

20. The method of Claim 18, wherein the conductive material comprises polysilicon, Si, or SiC.

21. The method of Claim 18, wherein the phase change material comprises a chalcogenide.

22. The method of Claim 21, wherein the phase change material comprises a binary, ternary or quaternary alloy.

23. The method of Claim 22, wherein the phase change material is selected from the group consisting of Ga Sb, In Sb, In Se, Sb2 Te3, Ge Te, Ge2Sb2Te5, In Sb Te, Ga Se Te, Sn Sb2 Te4, In Sb Ge, Ag In Sb Te, (Ge Sn)Sb Te, Ge Sb(Se Te), Te81Ge15Sb2S2 alloy, and combinations thereof.

24. The method of Claim 23, wherein the conductive material comprises polysilicon, Si, SiC, or other high bandgap and high thermal conductivity material.

25. The method of Claim 16, which further comprises:

forming a second generally planar IMD layer over the first IMD layer and the free surface of the phase change material; and

forming a second electrode in the second IMD layer and in contact with the free surface of the phase change material.

26. The method of Claim 25, wherein the interface, the phase change material and the second electrode are arranged so that a current path into the phase change material from the interface is generally parallel to the plane of the substrate and a current path out of the phase change material into the second electrode is generally normal to the plane of the substrate.

1 27. The method of Claim 26, wherein the first electrode receives the output of a transistor
2 formed in and on the substrate and in the ILD layer.

1 28. The method of Claim 27, wherein the second electrode is connectable to a voltage source.

29. An improved phase change memory cell fabricated by integrated circuit techniques on a substrate, the memory cell being of the type in which there is an interface between a layer of phase change material and a conductive element, the area of the interface determining the resistance thereof to current flow therethrough, wherein the improvement comprises:

the resistive element being a thin film of a conductive material that does not overlap, and extends away from, the phase change material layer in a direction generally parallel to the plane of the substrate, the resistance of the interface being determined by the thickness of the thin film normal to the substrate.

30. The memory cell of Claim 29, wherein the interface is defined by the engagement of a side of the phase change material layer and an end of the thin film, the side and the end being generally normal to the plane of the substrate.

31. The memory cell of Claim 29, wherein the conductive material comprises a high bandgap and high thermal conductivity material.

32. The memory cell of Claim 29, wherein heat produced by current through the interface flows from the interface into the phase change material layer in a direction generally parallel to the plane of the substrate.

33. The memory cell of Claim 29, the cell further being of the type in which current flows through the phase change layer from the interface to a contact on the phase change material layer, wherein:

current flows from the interface into the phase change material layer in a direction substantially parallel to the plane of the substrate; and

current flows from the phase change material layer into the contact in a direction generally normal to the plane of the substrate.

34. The memory cell of Claim 29, wherein:

the thin film resides on a dielectric stratum on the substrate; and

the phase change material layer resides in a trench formed in the stratum, the trench defining the length of the thin film toward the phase change material layer in a direction generally parallel to the plane of the substrate.

35. The memory cell of Claim 29, wherein the width of the thin film generally parallel to the plane of the substrate at the interface is determined by photolithography and the height of the thin film generally normal to the plane of the substrate at the interface is determined by thin film deposition parameters.

36. A memory cell, comprising:

a layer of phase change material; and

an elongated thin conductive film having one end engaging a side of the layer to define an interface having a width and a height, at least one dimension of the interface being determined non-photolithographically by thin film deposition parameters.

37. A method of using the memory cell of Claim 36, which comprises applying a voltage across the other end of the film and the layer so that current flows from the interface into the layer generally parallel to the film.

38. The method of Claim 37, wherein the current flows out of the layer generally normal to the film.